Electronic Version
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Claims

[c1] 1. A double-triggered silicon controlling rectifier, comprising:

a P-type substrate;

a first N-well region, formed within the P-type substrate;

a second N-well region, formed within the P-type substrate, and on one side of the first N-well region;

a third N-well region, formed within the P-type substrate, and on another side of the first N-well region, opposite to the second N-well region;

a plurality of N+ diffusion areas, comprising:

a first N+ diffusion area, formed in the first N-well region and coupled to an external power terminal;

a second N+ diffusion area, formed in the first N-well region and on one side of the first N+ diffusion area, as a N-type trigger terminal of the double-triggered silicon controlling rectifier;

a third N+ diffusion area, formed in the first N-well region and on another side of the first N+ diffusion area, opposite to the second N+ diffusion area as the N-type trigger terminal of the double-triggered silicon controlling rectifier;

a fourth N+ diffusion area, partially formed in the third

N-well region and partially formed in the P-type substrate, and on one side of the second N+ diffusion region, opposite to the first N+ diffusion region as a cathode of the double-triggered silicon controlling rectifier; and

a fifth N+ diffusion, partially formed in the third N-well region and partially formed in the P-type substrate, and on one side of the third N+ diffusion region, opposite to the first N+ diffusion region as the cathode of the double-triggered silicon controlling rectifier;

a plurality of P+ diffusion areas, comprising:

a first P+ diffusion area, formed within the first N-well region and between the first N+ diffusion area and the second N+ diffusion area, as an anode of the double-triggered silicon controlling rectifier;

a second P+ diffusion area, formed within the first N-well region and between the first N+ diffusion area and the third N+ diffusion area, as the anode of the double-triggered silicon controlling rectifier;

a third P+ diffusion area, formed within the P-type substrate between the first and the third N-well regions, and between the second and the fourth N+ diffusion areas, as a P-type trigger terminal of the double-triggered silicon controlling rectifier;

a fourth P+ diffusion area, formed within the P-type substrate between the first and the second N-well re-

gions, and between the third and the fifth N+ diffusion areas, as the P-type trigger terminal of the double-triggered silicon controlling rectifier;

a fifth P+ diffusion area, formed within the P-type substrate and on one side of the fourth N+ diffusion area, opposite to the third P+ diffusion area, as a ground terminal of the double-triggered silicon controlling rectifier; and

a sixth P+ diffusion area, formed within the P-type substrate and on one side of the fifth N+ diffusion area, opposite to the fourth P+ diffusion area, as the ground terminal of the double-triggered silicon controlling rectifier; and

a plurality of isolation structures, formed within the P-type substrate and between spaces of the pluralities of N+ and P+ diffusion areas.

[c2] 2. The double-triggered silicon controlling rectifier of claim 1, wherein the isolation structures comprise shallow trench isolation structures.

[c3] 3. The double-triggered silicon controlling rectifier of claim 2, wherein a depth of the shallow trench isolation structure is about 0.4 μm for a 0.25-μm complementary metal-oxide-semiconductor (CMOS) process.

[c4] 4. The double-triggered silicon controlling rectifier of

claim 1, wherein a portion of the isolation structures comprise dummy gate terminals.

[c5] 5. The double-triggered silicon controlling rectifier of claim 4, wherein the dummy gate terminal is made from polycrystal material.

[c6] 6. The double-triggered silicon controlling rectifier of claim 1, depths of the N+ and P+ diffusion areas are about 0.18 μm for a 0.25-μm complementary metal-oxide-semiconductor (CMOS).

[c7] 7. An electrostatic discharge (ESD) protection circuit using a double-triggered silicon controlling rectifier, fabricated in an integrate circuit and disposed between an input/output (I/O) pad and an internal circuit thereof, the ESD protection circuit comprising:
a first double-triggered silicon controlling rectifying module, having a first terminal, a second terminal, a N-type trigger terminal and a P-type trigger terminal, the first terminal coupled to a high-voltage external power terminal, the second terminal coupled to the I/O pad and the internal circuit of integrate circuit;
a first electrostatic detecting module, having a first output terminal, a second output terminal, a first input terminal and a second input terminal, the first output terminal coupled to the first N-type trigger terminal, the

second output terminal coupled to the first P-type trigger terminal, the first input terminal coupled to the high-voltage external terminal, the second input terminal coupled to the internal circuit of the integrate circuit and the I/O pad, wherein when a negative ESD voltage attacks the I/O pad, the first double-triggered silicon controlling rectifying module directs ESD current from the first N-type trigger terminal to the first electrostatic detecting module and directs ESD current from the second output terminal to the first double-triggered silicon controlling rectifying module;

a second double-triggered silicon controlling rectifying module, having a third terminal, a fourth terminal, a second N-type trigger terminal and a second P-type trigger terminal, the third terminal coupled to the I/O pad and the internal circuit of the integrate circuit, the second terminal coupled to a low-voltage external power terminal; and

a second electrostatic detecting module, having a third output terminal, a fourth output terminal, a third input terminal and a fourth input terminal, the third output terminal coupled to the second N-type trigger terminal, the fourth output terminal coupled to the second P-type trigger terminal, the third input terminal coupled to the internal circuit of the integrate circuit and the I/O pad, the fourth input pad coupled to the low-voltage external

power terminal, wherein when a positive ESD voltage attacks the I/O pad, the second double-triggered silicon controlling rectifying module directs ESD current form the second N-type trigger terminal to the second electrostatic detecting module, and the directs ESD current from the fourth output terminal to the second double-triggered silicon controlling rectifying module.

[c8] 8. The ESD protection circuit using a double-triggered silicon controlling rectifier of claim 7, wherein the first double-triggered silicon controlling rectifying module comprises:

a first double-triggered silicon controlling rectifier, having an anode, a cathode, N-type trigger terminal and the P-type trigger terminal, the anode of the first double-triggered silicon controlling rectifier serving as the first terminal; and

a second double-triggered silicon controlling rectifier, having an anode, cathode, a N-type trigger terminal and a P-type trigger terminal, the anode of the second double-triggered silicon controlling rectifier coupled to the cathode of the first double-triggered silicon controlling rectifier, the cathode of the second double-triggered silicon controlling rectifier serving as the second terminal, the N-type trigger terminal of the second double-triggered silicon controlling rectifier coupled to the N-type

trigger terminal of the first double-triggered silicon controlling rectifier serving as the first N-type trigger terminal, the P-type trigger terminal of the second double-triggered silicon controlling rectifier coupled to the P-type trigger terminal of the first double-triggered silicon controlling rectifier serving as the first P-type trigger terminal.

[c9] 9. The ESD protection circuit using a double-triggered silicon controlling rectifier of claim 7, wherein the second double-triggered silicon controlling rectifying module comprises:

a third double-triggered silicon controlling rectifier, having an anode, a cathode, a N-type trigger terminal and a P-type trigger terminal, the anode of the third double-triggered silicon controlling rectifier serving as the third terminal; and

a fourth double-triggered silicon controlling rectifier, having an anode, cathode, a N-type trigger terminal and a P-type trigger terminal, the anode of the fourth double-triggered silicon controlling rectifier coupled to the cathode of the third double-triggered silicon controlling rectifier, the cathode of the fourth double-triggered silicon controlling rectifier serving as the fourth terminal, the N-type trigger terminal of the fourth double-triggered silicon controlling rectifier coupled to the N-type

trigger terminal of the third double-triggered silicon controlling rectifier serving as the second N-type trigger terminal, the P-type trigger terminal of the fourth double-triggered silicon controlling rectifier coupled to the P-type trigger terminal of the third double-triggered silicon controlling rectifier serving as the second P-type trigger terminal.

[c10] 10. The ESD protection circuit using a double-triggered silicon controlling rectifier of claim 7, wherein the first electrostatic detecting module comprises:
a first N-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the first N-type transistor coupled to the first input terminal, the second source/drain terminal serving as the second output terminal of the first N-type transistor, the gate terminal of the first N-type transistor coupled to the first input terminal and grounded, the base terminal of the first N-type transistor grounded; and
a s N-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the second N-type transistor serving as the first output terminal, the second source/drain terminal of the second N-type transistor coupled to the second input terminal,

the gate terminal of the second N-type transistor coupled to the gate terminal of the first N-type transistor, the base terminal of the second N-type transistor grounded.

[c11] 11. The ESD protection circuit using a double-triggered silicon controlling rectifier of claim 7, wherein the first electrostatic detecting module comprises:
a first P-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the first P-type transistor coupled to the first input terminal, the second source/drain terminal of the first P-type transistor serving as the second output terminal, the gate terminal of the first P-type transistor coupled to the first input terminal and the second input terminal, the base terminal of the first P-type transistor coupled to the first input terminal; and
a second P-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the second P-type transistor serving as the first output terminal, the second source/drain terminal of the second P-type transistor coupled to the second input terminal, the gate terminal of the second P-type transistor coupled to the gate terminal of the first P-type transistor,

the base terminal of the second P-type transistor coupled to the first input terminal.

[c12] 12. The ESD protection circuit using a double-triggered silicon controlling rectifier of claim 7, wherein the second electrostatic detecting module comprises:
a third P-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the third P-type transistor coupled to the third input terminal, the second source/drain terminal of the third P-type transistor as the fourth output terminal, the gate terminal of the third P-type transistor coupled to the high-voltage external power terminal and the fourth input terminal, the base terminal of the third P-type transistor coupled to the high-voltage external power terminal; and
a fourth P-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the fourth P-type transistor as the third output terminal, the second source/drain terminal of the fourth P-type transistor coupled to the fourth input terminal, the gate terminal of the fourth P-type transistor coupled to the gate terminal of the third P-type transistor, the base terminal of the fourth P-type transistor coupled to the

high-voltage external power terminal.

[c13] 13. The ESD protection circuit using a double-triggered silicon controlling rectifier of claim 7, wherein the second electrostatic detecting module comprises:
a third N-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the third N-type transistor coupled to the third input terminal, the second source/drain terminal of the third P-type transistor serving as the fourth output terminal, the gate terminal of the third P-type transistor coupled to the third input terminal and the fourth input terminal, the base terminal of the third N-type transistor grounded; and
a fourth N-type transistor having a first source/drain terminal, a second source/drain terminal, a gate terminal and a base terminal, the first source/drain terminal of the fourth N-type transistor serving as the third output terminal, the second source/drain terminal of the fourth N-type transistor coupled to the fourth input terminal, the gate terminal of the fourth N-type transistor coupled to the gate terminal of the third N-type transistor, the base terminal of the fourth N-type transistor coupled to the fourth input terminal.